Session 9 Overview

Clocking

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The job of the clock designer in a large digital chip is increasingly challenging. The designer is faced with the competing requirements of increasing clock frequency and clock distribution area, reducing skew, jitter, and power dissipation, all while adding testability and reliability features. Furthermore, recent design trends in digital chips use variable supply voltages and operating frequencies to achieve multiple power/performance envelopes to enable products that simultaneously address different market segments. These requirements place additional burdens on the clocking system, especially on the clock generation mechanism.

Although traditional analog PLLs have very good jitter performance, they are not versatile enough for these applications in terms of power supply and tuning range. Moreover, migration to more advanced process nodes with higher-leakage devices requires challenging and time-consuming redesign of analog circuits. Going all-digital addresses the issues of process migration, supply voltage versatility and wide dynamic range. But can an all-digital clock generator ever approach the jitter performance of an analog one? Can we build an all-digital clock generator that reaches 40GHz? There are three papers in this session that provide concrete answers to these questions.

Despite their problems and limitations, traditional balanced-tree-based clock distributions are not going away any time soon since they are robust and well-understood. Over the past few years, this conference has presented alternative distribution methods based on traveling rotary waves, standing waves and LC resonance. Although the feasibility of such distribution schemes for a large digital chip is yet unproven, their benefits are hard to ignore. The benefits include lower power dissipation from energy recycling, reduced jitter due to LC filtering, limited buffering and controlled skew due to the predictability of electromagnetic wave properties. Two papers in this session advance the state-of-the-art in LC techniques. Finally, two papers present interesting digital phase-locking techniques with a wide application range.

Paper 9.1 from IBM presents an all-digital PLL (ADPLL) with a 0.5V-to-1.3V supply range and 500MHz-to-8GHz output frequency range. The ADPLL uses an inverter-array structure as a VCO, which has a wide and linear tuning curve. The achieved period jitter is 0.7ps rms, good enough for very demanding digital applications. The design follows the trend of multiple power/performance operating points dissipating 8mW/GHz at 1.2V and 1.6mW/GHz at 0.5V. Clock multiplying DLLs are a well-known technique for delay-line-based clock generation. Paper 9.4 from NTU takes this concept to the next level by using this structure to generate a 40GHz output clock in 90nm CMOS. The authors solve the coarse delay resolution problem by phase locking the delay line to multiple clock periods and using equivalent phases from different periods to feed an LC-tank based oscillator. Paper 9.2 from NEC is also a clock-multiplying DLL using a multiplexer-based edge interleaver as the clock multiplier. The edge interleaver, along with dithering techniques, enables high resolution control of both rising and falling edges that makes this system appropriate for testing timing margins.

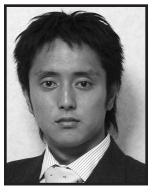
Paper 9.5 from Hiroshima U and Elpida presents a standing-wave clock oscillator that solves the issue of diminishing clock amplitude along the length of the transmission line by using inductive loading. Multiple such oscillators are synchronized and form an entire distribution scheme by magnetic coupling. Paper 9.6 from UCLA presents an LC-based clock distribution that trades off input versus clock buffer jitter. This adaptive scheme achieves power reduction while maintaining low jitter by adaptively adjusting the ratio between the LC-resonant buffer and the injection-locked oscillator.

Paper 9.3 from Harvard U describes a digital technique for static phase offset reduction in a PLL. It can be used in applications where a small offset between reference and output clock is desired, and as an added benefit the reference spur is reduced. Paper 9.7 from Korea U and Hynix presents an interesting open loop DLL based on replica delays. It has a fast lock time, wide dynamic range and includes duty-cycle correction.

9.1 A Wide Power-Supply Range (0.5-to-1.3V) Wide Tuning-Range (500MHz-to-8GHz) All-Static CMOS ADPLL in 65nm SOI **8:30 AM**

J. Tierno, IBM T.J. Watson, Yorktown Heights, NY

An all-static CMOS 65nm SOI ADPLL has a fully programmable loop filter and a 3rd-order ΔΣ modulator. The DCO is a 3-stage, static-inverter-based ring-oscillator programmable in 768 frequency steps. The ADPLL locks from 500MHz to 8GHz at 1.3V 25°C, and 90MHz to 1.2GHz at 0.5V 100°C. The area is 200×150μm² and it dissipates 8mW/GHz at 1.2V and 1.6mW/GHz at 0.5V. The synthesized 4GHz clock has period jitter of $0.7ps_{rms}$, and long-term jitter of $6ps_{rms}$. The phase noise is –110dBc/Hz at 10MHz offset.



9.2 A 1-to-2GHz 4-Phase On-Chip Clock Generator with Timing-Margin Test Capability **9:00 AM**

S. Kaeriyama, NEC, Sagamihara, Japan

A clock generator fabricated in 90nm CMOS occupies 300×128μm² die area and dissipates 40mW at 1.2V. An interleaved clock-edge control technique extends the frequency tuning range and enables control of both rising and falling edge timing. A clock-period dithering technique enhances frequency tuning resolution. Disturbance-control functions that control jitter, duty cycle, and clock skew make timing margin testing possible.

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9.3 All-Digital Dynamic Self-Detection and Self-Compensation of Static Phase Offsets in Charge-Pump PLLs **9:30 AM**

Y. Liu, Harvard University, Cambridge, MA

A 90nm CMOS charge-pump PLL incorporates an all-digital auxiliary feedback loop that dynamically detects and compensates the static phase offset. The on-chip monitoring of the static phase offset with a preset target value allows for accurate and reliable compensation. A measured static phase offset as large as 600ps is compensated to a ±15ps range.

9.4 A 40GHz DLL-Based Clock Generator in 90nm CMOS Technology **10:15 AM**

C-N. Chuang, National Taiwan University, Taipei, Taiwan

A 2-to-5GHz multi-phase multi-period-locked DLL is fabricated in a 90nm CMOS technology. At 5GHz, the measured rms jitter is 0.874ps and the peak-to-peak jitter is 7.56ps. The multi-phase DLL is used for a 40GHz clock generator. The core area is 0.374×0.326mm² and the power consumption is 45mW at 1V.

9.5 12GHz Low-Area-Overhead Standing-Wave Clock Distribution with Inductively-Loaded and Coupled Technique **10:45 AM**

M. Sasaki, Hiroshima University, Hiroshima, Japan

A clock distribution network using inductively-loaded standing-wave oscillators is designed. Synchronization among oscillators is achieved through magnetic coupling. The 12GHz clock distribution network is prototyped in a 6M 0.18μm CMOS technology. A peak-to-peak jitter of 4.7ps is achieved on a 5×5 mesh structure, with a pitch of 200μm. The power consumption is 80mW at 0.9V.

9.6 Adaptive Low-Jitter LC-Based Clock Distribution **11:15 AM**

L-M. Lee, University of California, Los Angeles, CA

A low-jitter LC-based clock distribution in 0.13μm CMOS uses a frequency-tuning technique based on a voltage-swing digitizer. Optimum jitter performance is achieved by adaptively adjusting the injection-lock ratio. The efficiency of this technique results in 25% power-savings in the clock buffer for similar or better jitter performance.

9.7 A 7ps-Jitter 0.053mm² Fast-Lock ADDLL with Wide-Range and High-Resolution All-Digital DCC **11:45 AM**

D. Shin, Korea University, Seoul, Korea

An ADDLL is designed to achieve low jitter, fast lock time and nearly 50% duty cycle with an open-loop duty-cycle corrector. The ADDLL operates over a frequency range from 440MHz to 1.5GHz with 15 cycles of maximum lock-in time and occupies 0.053mm² in 0.18μm 1.8V CMOS. The peak-to-peak jitter is 7ps at 1.5GHz and the power consumption is 43mW.